Agilent HPFC-5400 Tachyon DX2 Dual Channel Fibre Channel IC

Product Overview

Product Description

The Tachyon DX2 is a high-performance PCI/PCI-X native dual 1 and 2 gigabit/sec Fibre Channel controller for host bus adapters and embedded sub-systems.

DX2 is the fourth member of the Agilent Technologies family of Fibre Channel interface controllers. It provides the performance enhancing features of PCI-X and is a single chip solution that offers the most economical component cost savings.

The DX2 interfaces directly to an industry standard PCI/PCI-X bus. Each channel can be independently configured to use either an HSPI-compatible 10-bit external SERDES or to use the internal SERDES.

Applications

- **Embedded subsystems**
- **Disk arrays**
- **SCSI bridge**
- **High performance host bus adapters**

Features

- **Dual channel Fibre Channel operation on one chip for the lowest overall FC solution costs**
- **Full duplex operation for each channel**
- **Concurrent for each dual channel operation at full link rate**
- **1 and 2 gigabit Fibre Channel operation support via internal transceivers or external HSPI-compatible transceivers (SERDES)**
- **Dual function industry standard 33/66 MHz PCI or 66/100/133 MHz PCI-X backplane interface with 32/64 bit support**
- **3.3V PCI/PCI-X I/O**
- **Compliance to PCI Local bus Specification, Rev 2.2**
- **MSI (Message Signaled Interrupt) support**
- **Compliance to PCI-X Addendum, Rev 1.0A**
- **PCI/PCI-X hot plug compatible**
- **Output impedance control on PCI-X I/O for point-to-point or multi-point connectivity**
- **Eight GPIO pins per channel**
- **Loss of signal indication (per channel) during internal serdes mode**
- **Multiple split read transaction support on PCI-X**
- **No external SRAM required for operation**
- **4K on chip boot RAM**
- **Supports fabric, point-to-point (N_Port) and loop (Public and Private) topologies**
- **Optional external boot ROM/Flash (128K Bytes)**
- **Eight full-frame inbound buffers and four full-frame outbound buffers per FC channel**
- **State machine processing of inbound and outbound data**
- **Fully assisted Class 2 and Class 3 FCP with simultaneous initiator and target functionality**
- **Provision to support auto-speed negotiation in TSDK software**
- **Full byte-level parity protection on internal data path and RAM**
- **Backwards compatible to Tachyon XL2 programming interface**
- **Supports ACK_0 and ACK_1 models in hardware**
- **Complete sequence segmentation and reassembly done in hardware**
- **64-bit addressing (44/45 bits per Length/Address pair)**
- **Mechanisms to reduce number of interrupts generated by the adapter to help reduce the software overhead required to support the adapter**
- **Frame payload size up to 2048 bytes**
- **Loop map, broadcast, directed reset and bypass support**
- **Non-zero login BB_Credit support**
- **Compliance with FC-AL-2 ANSI Standard**
- **Compliance with Hardware Design Guide for Microsoft Windows NT Server, Version 2.0**
- **Compatible with ACPI/Power Management Specification**
- **Minimal board space required**

Agilent Technologies

Tachyon DX2 Architecture

The Tachyon DX2 advances the Tachyon XL2 architecture, providing a complete hardware-based solution in a dual channel Fibre Channel device. The DX2 offers full duplex capability within each channel as well as full performance.

In addition, the DX2 has numerous independent functional blocks which concurrently process inbound data, outbound data, control and commands in hardware. This results in the lowest latency and highest performance in a multi-function device.

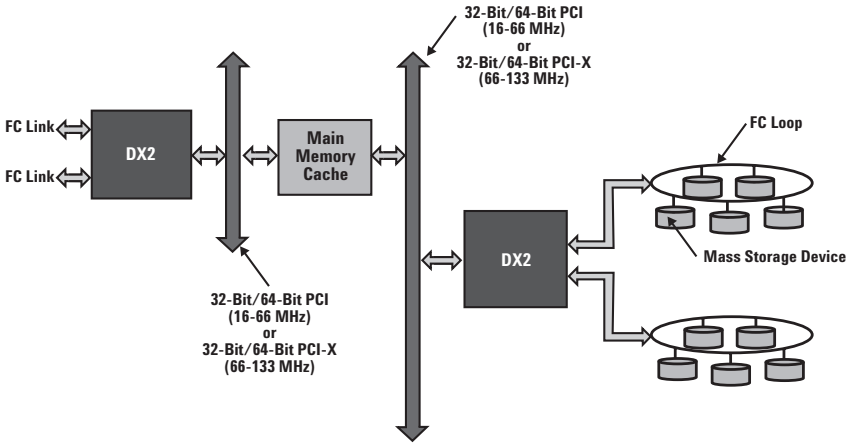

Figure 1.

Typical Subsystem Application

Figure 1 shows DX2 in an optional high-performance configuration.

The DX2 chips interface between the mass storage devices on the Fibre Channel loops, the main memory of the subsystem and the host.

In this example, the DX2 chips interface with main memory cache through 33/66 MHz PCI or 66/100/133 MHz PCI-X backplane, with 32/64-bit support in either mode.

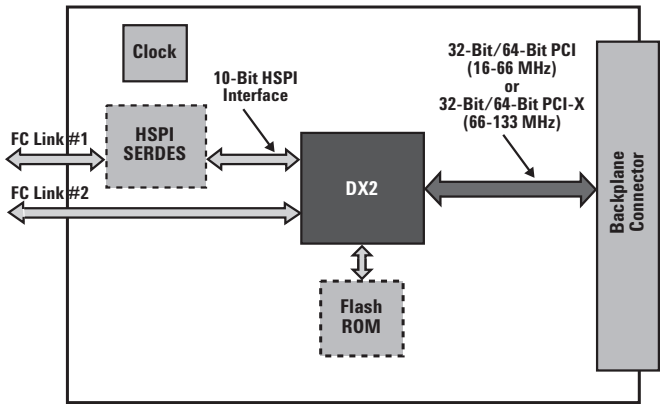

Figure 2.

Host Bus Adapter Example

Figure 2 shows an example of a DX2 on a generic host bus adapter.

On the backplane, the DX2 interfaces directly to an industry standard 33/66 MHz PCI or 66/100/133 MHz PCI-X bus. On the frontplane, each channel can be independently configured to use either an HSPI-compatible 10-bit external SERDES or an integrated SERDES.

The onboard optional boot ROM/Flash ROM is connected directly to the DX2 chip.

For product information and a complete list of Agilent contacts and distributors, please go to our web site.

www.agilent.com/semiconductors

E-mail: SemiconductorSupport@agilent.com

Obsoletes 5988-9182EN
April 28, 2003
5988-9437EN

Agilent Technologies